CLAIMS

What is claimed is:

1. (currently amended) A structure comprising:

a shaped clock signal generator means and receiver input port for receiving data signal at a bit rate said shaped clock generator being synchronous or asynchronous with the data bit rate received by [[a]] said data signal receive input port; and

a data signal receiver port and processor for providing control signal generation means for selecting the said shaped clock signal for further transmission and/or modulation.

2. (currently amended) A structure comprising:

a splitter receiving an input signal and splitting said input signal into two ~~or more~~ signal streams;

a clock generator for receiving ~~one of~~ the said signal streams and generating [[a]] two shaped clock signals;

~~one or more shaped clock generator means for receiving said clock signal and for generation of one or more shaped clock signals;~~

~~a set of input ports for receiving shaped clock signals;~~

processor means for generation of data-based selection control signals;

a selector switch for selecting one of the two shaped clock signals, said selector switch having an input interface port connected to the data-based selection control signals and another set of input ports connected to the shaped clock signals; and

an output interface port coupled to said selector switch output.

3. (currently amended) An architecture comprising:

a data interface input for receiving input data and for providing an input data-based clock selector data signal;

~~a set of~~ two input ports for receiving ~~a set of~~ two ~~shaped clock signals and of~~ not-shaped clock signals;

~~a set of one or more~~ two clock generators which differ in one or more clock parameters from each other;

two processors for processing clock signals;

a selector switch for selecting one of the processed clock signals; [[and]]

a transmitter circuit for transmitting one or more of the selected clock signals; and

a data interface output port for receiving said selected clock signals and providing ~~it~~ them to the transmitter circuitry.

4. (currently amended) A structure comprising:

a clock generator which provides clock signals to two or more clock transition time shifting ~~and~~ or clock shaping signal generators;

generation and switching means for generation and selection of clock transition time shifting or clock shaped signals;

~~a data input port and connection to a data input interface input encoder for the generation of clock selector data signal by said data input interface encoder;~~

a switch to choose, ~~based on said clock selector data signal,~~ one of the clock shaped or transition time-shifted shaped clock signals and connect the selected clock signal to the data interface output unit . [[; and]]

~~a data interface output unit for connecting the selected signal to the transmission medium or further signal processing.~~

5. (currently amended) A transmit signal processor structure comprising:

a first clock shaped signal generator having a first set of clock shaping parameters;

a second clock shaped signal generator having a second set of clock shaping parameters, said second set of clock shaping parameters having at least one parameter different from that of the first set of clock signal shaping parameters;

a data input receive circuitry and processor for selection of one of the said first or second clock shaped signals;

a switch for switching between the first set and second set of shaped clock parameters; and

an output interface port to provide the selected signal to the ~~transmission medium.~~ output of the transmit signal processor.

6. (currently amended) A ~~spectral saving~~ data and clock signal processing system comprising:

an input interface circuitry for receiving data from a data signal source;

data signal and clock signal processing means to provide a clock modulated signal having changeable distances between the rising edges and falling edges of the modulated clock signals; and

control means having its input connected to the data signal source and its output connected to edge distance switch selection means; and

~~digital~~ interface output means to connect the clock modulated signal to the output ~~interface~~ of the ~~subsequent signal processor.~~ clock signal processing system.

7. (currently amended) A clock signal modulator comprising:

a data input interface means to provide data signals to an asynchronous pure clock source;

an asynchronous pure clock generator means to provide a pure clock signal; ~~and~~

a clock modulator device for providing a clock modulated signal; and

a selector switch means which is controlled by the data interface to provide a shorter distance between the falling edge and rising edge of the clock modulated signal for a zero state data signal and a longer distance between the falling edge and rising edge of the clock modulated signal for a one-state data signal.

8. (currently amended) A clock converter system comprised of:

a clock converter input interface processor unit for providing and selecting input shaped clock signals;

clock signal selection means;

an input data interface means for controlling the selection process of the shaped clock signals ~~which is provided to the interface output unit means~~ ;

a clock signal shaping means to provide smoothed continuous clock signals to the clock signal selection means having one or more different clock signal parameters; and

an output signal processor for processing ~~means to accept~~ the smoothed different clock signal parameter processed clock converted signals.
converted signals.

9. (currently amended) A clock modulated signaling system comprising:

an input data interface means to provide control signal generation and selection means of shaped clock signals;

a quadrature modulator for quadrature modulating the shaped clock baseband signal;

an interface means to provide signal processing means for modulating the clock modulated baseband signal by means of a cross-correlated quadrature modulator system;

an output amplifier means to connect the cross-correlated quadrature modulated signal to the ~~transmission medium~~ demodulator;

demodulation means to demodulate the received quadrature modulated signal; and

signal processor means to decode and regenerate the shaped clock ~~modulated~~ signals.

10. (currently amended) An architecture comprising:

a data interface input for receiving input data and for providing an input data- based clock selector data signal;

~~a set of~~ two input ports for receiving ~~a set of~~ two shaped clock signals ~~and of not shaped clock signals~~ ;

two processors for processing said clock signals;

~~a set of one or more~~ two clock generators which differ from each other in one or more clock parameters;

a selector switch for selecting one of the processed clock signals; ~~and~~

a transmitter circuit for transmitting one of the selected clock signals; and

a data interface output port for receiving said selected clock signals and providing ~~it~~ them to the transmitter circuitry.

11. (original) A method comprising steps:

receiving a data signal;

generating a shaped clock signal in response to said received data signal;

generating a control signal for selecting said generated shaped clock signal; and

processing said selected shaped clock signal for transmission or modulation.

12. (original) The method in claim 11, wherein said shaped clock signal is generated synchronously with a data bit rate of said received data signal.

13. (original) The method in claim 11, wherein said shaped clock signal is generated asynchronously with a data bit rate of said received data signal.

14. (original) A method of signaling using clock modulated signals, said method comprising:

selecting at least one shaped clock signal;

cross-correlating and quadrature modulating said selected at least one shaped clock signal;

amplifying said cross-correlated quadrature modulated signal;

transmitting said amplified cross-correlated quadrature modulated signal;

receiving said transmitted amplified cross-correlated quadrature modulated signal;

demodulating said received signal; and

decoding said received demodulated signal and regenerating said clock signal.